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(54) **High speed, nonvolatile, electrically erasable memory system.**

(57) A method is disclosed for encoding binary data into an electrically erasable memory, said memory comprising a matrix of memory cells, each of said cells comprising a floating gate field effect pMOS transistor for storage of binary data and an npn bipolar transistor for selective access to stored data. The control gate of each storage transistor in a row is connected to an X write line; the emitter of each bipolar transistor in a row is connected to an X sense line; the source of each bipolar transistor in a row is connected to a source line and the collector of each bipolar transistor in a column is connected to a Y sense line. The method comprises:

(a) applying an erase voltage to each of said Y sense lines and, simultaneously, maintaining each of said X sense lines at said erase voltage, maintaining each of said X write lines at ground and applying said erase voltage to each of said source lines such that each of said storage transistors assumes a relatively negative threshold state; and

(b) applying a write voltage to selected X write lines while maintaining unselected X write lines at ground, and, simultaneously, maintaining selected Y sense lines at ground and unselected Y sense lines at an inhibit voltage which is less than said write voltage and maintaining each of said X sense lines at an intermediate voltage which is equal to or less than the base/emitter breakdown voltage of said bipolar transistors such that the storage transistors of memory cells located at the intersections of said selected X write lines and said selected Y sense lines assume a relatively positive threshold state.

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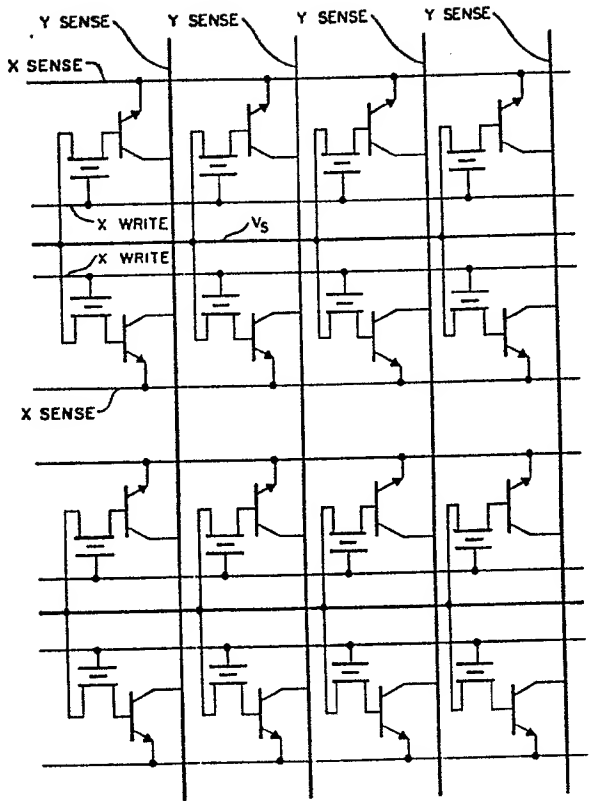
Y SENSE
Y SENSE
Y SENSE
Y SENSE
X SENSE
X WRITE
V_S
X WRITE
X SENSE

FIG. 3

HIGH SPEED, NONVOLATILE, ELECTRICALLY ERASABLE MEMORY SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to electrically erasable memory systems and in particular to a method for encoding binary data into a nonvolatile, electrically erasable memory system.

Prior art nonvolatile memory systems have been restricted to field effect transistor, typically MOS, technology with a resultant limitation in operating speed. While it is well known that higher operating speeds are provided by bipolar technology, prior bipolar art has lacked a nonvolatile storage mechanism.

The present invention provides a method for high speed erasing, writing and reading binary data in an electrically erasable nonvolatile memory array.

SUMMARY OF THE INVENTION

According to a preferred embodiment of the present invention, a method for encoding binary data into an electrically erasable memory is provided, said memory comprising a matrix of memory cells.

Each cell of the memory array comprises a pMOS floating gate transistor for data storage and a merged npn bipolar transistor for selective access to stored data. The pMOS floating gate transistor acts similarly to a current source, injecting (depending on its threshold) either finite or zero base current into the npn bipolar transistor, causing the bipolar transistor to exhibit either high or low impedance.

The memory array comprises a matrix of such memory cells formed as a plurality of rows and a plurality of columns. A plurality of X write lines are provided, the control gate of each pMOS storage transistor in a row of memory cells being connected to an X write line corresponding to that row. A plurality of X sense lines are also provided, the emitter of each bipolar transistor in a row of cells being connected to an X sense line corresponding to that row. A plurality of source lines are also provided, the source of each pMOS storage transistor in a row of cells being connected to a source line corresponding to that row. A plurality of Y sense lines are also provided, the collector of each bipolar transistor in a column of cells being connected to a Y sense line corresponding to that column. In a preferred embodiment, continuous strips of N+ buried layer form the Y sense lines and are OR-tied to the collectors of the bipolar transistors in the corresponding column.

Binary data is encoded into the memory array by applying an erase voltage to each of the Y sense lines in the array, and, simultaneously, maintaining each of the X sense lines at the erase voltage. At the same time, each of the X write lines is maintained at ground and the erase voltage is applied to each of the source lines. This condition causes each of the storage transistors to assume a relatively negative threshold state. Next, a write voltage is applied to selected X write lines while unselected X write lines are maintained at ground. Simultaneously, selected Y sense lines are maintained at ground and an inhibit voltage which is less than the write voltage is applied to unselected Y sense lines. At the same time, each of the X sense lines in the array is maintained at an intermediate voltage which is less than or equal to the base/emitter breakdown voltage of the bipolar transistors.

These conditions cause the pMOS storage transistors of the memory cells located at the intersections of the selected X write lines and the selected Y sense lines to assume a relatively positive threshold state.

To read binary data from the array, a selected X sense line is maintained at ground while unselected X sense lines and each Y sense line are maintained at about +3 volts. At these conditions, memory cells connected to the selected X sense lines and having pMOS storage transistors in the relatively negative threshold state are less conducting than memory cells connected to the selected X sense line and having storage transistors in the relatively high threshold state. The memory cells connected to the selected X sense line are then monitored to determine their relative conductance.

A BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit schematic for a memory cell used in the method of the present invention;

Fig. 2 is a topographical layout of a 4 X 4 memory array used in the method of the present invention;

Fig. 3 is a circuit schematic of the memory array shown in Fig. 2; and

Fig. 4 is a cross-sectional view taken along line 4-4 in Fig. 2.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

As shown in Fig. 1, a preferred embodiment of a high speed nonvolatile memory cell of the invention comprises a floating gate pMOS transistor for data storage and a merged npn bipolar transistor for selective access to stored data. A first N+ polysilicon region forms the floating gate 22a of the pMOS storage transistor while a first P+ polysilicon region forms its control gate 26a. A second region of N+ polysilicon forms the emitter 22b of the npn bipolar transistor. A second region of P+ polysilicon forms the contact 26b to P+ epitaxial regions which form part of the base of the npn bipolar transistor. The N+ buried layer 13 serves as the collector of the bipolar transistor.

A process for fabricating a semiconductor memory cell structure, the circuit schematic for which is shown in Fig. 1, and the memory cell structure which results from this process are disclosed in European patent application 81402036.8 published with No. 0055182 from which the present patent application is divided.

The memory cell shown in Fig. 1 is utilized in an electrically erasable, high speed, nonvolatile memory array such as that shown in Figs. 2-4.

As shown in Figs. 2-3, the memory array comprises a matrix of memory cells of the type described above which are formed as a plurality of rows and a plurality of columns of such cells. Fig. 2 shows a section of the memory array topography, representing 16 bits in a 4 X 4 array.

The memory array includes a plurality of X write lines, the control gate of each pMOS storage transistor in a row of memory cells being connected to an X write line corresponding to that row. In the illustrated embodiment, the X write line comprises P+ polysilicon and forms the control gate of the pMOS transistors in that row.

The array further includes a plurality of X sense lines, the emitter of each bipolar transistor in a row of cells being connected to an X sense line corresponding to that row. In the illustrated embodiment, the X sense line comprises N+ polysilicon and links all emitters of the npn bipolar transistors in the row.

The array further comprises a plurality of source lines, the source of each pMOS storage transistor in a row of cells being connected to a source line corresponding to that row.

The array further includes a plurality of Y sense lines, the collector of each npn bipolar transistor in a column of memory cells being connected to a Y sense line corresponding to that column. In the illustrated embodiment, orthogonal strips of N+ buried layer form the Y sense lines and are OR-tied to the collectors of the npn bipolar transistors.

To encode binary data into the memory, an erase voltage, preferabley about +20 volts, is applied to each of the Y sense lines. Simultaneously, each of the X sense lines is maintained at the erase voltage, each of the X write lines is maintained at ground and the erase voltage is applied to each of the source lines. At these conditions, each of the storage transistors in the array assumes a relatively negative threshold state. A memory cell having a relatively negative threshold state is relatively less

conducting when a read voltage is applied. Next, a write voltage, preferably about +20 volts, is applied to selected X write lines while maintaining unselected X write lines at ground. Simultaneously, selected Y sense lines are maintained at ground and an inhibit voltage, preferably about +5 volts, is applied to unselected Y sense lines. The inhibit voltage inhibits threshold shift by reducing the field across the thin oxide beneath the floating gate of the pMOS storage transistor. The inhibit voltage is insufficient to cause any significant threshold disturbance in unselected devices over many cycles of data change. At the same time, each of the X sense lines is maintained at an intermediate voltage, which intermediate voltage is between the write voltage and the inhibit voltage and preferably is about +10 volts. The intermediate voltage is equal to or less than the base/emitter breakdown voltage of the npn bipolar transistors in the array. At these conditions, the pMOS storage transistors of memory cells located at the intersections of selected X write lines and selected Y sense lines assume a relatively positive threshold state while the remaining memory cells remain at the relatively negative threshold state. A memory cell in a relatively positive threshold state is relatively more conducting when a read voltage is applied.

To read data from the memory, a selected X sense line is maintained at ground. Simultaneously, unselected X sense lines and each of the Y sense lines are maintained at about +3 to +5 volts. At these conditions, memory cells connected to the selected X sense line and having pMOS storage transistors in the relatively negative threshold state are less conducting than memory cells connected to the selected X sense line and having pMOS storage transistors in the relatively positive threshold state. Memory cells connected to the selected X sense lines are monitored to determine their relative conductance.

Table I provides a summary of operating conditions for the array.

Mode	READ				WRITE				ERASE
Axes Selected	X Y	Yes Yes	Yes No	No Yes	No No	Yes Yes	Yes No	No Yes	No No	All All
Control Line	Unit									
Xsense	V	0	0	3	3	5	5	5	5	20
Ysense	V	3	don't care	3	3	0 or 10	V_{W1}=10	V_{W1}=10	V_{W1}=10	20
Xwrite	V	3	3	3	3	V_W=20	V_W=20	0	0	0
V_S	V	3	3	3	3					20
Ysense read 1	μA	100					N/A			N/A
Ysense read 0	μA	0								

TABLE 1 TYPICAL OPERATING CONDITIONS

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CLAIMS

1. A method for encoding binary data into an electrically erasable memory, said memory comprising a matrix of memory cells formed as a plurality of rows and a plurality of columns of said cells each of said cells comprising a floating gate field effect pMOS transistor for storage of binary data and an npn bipolar transistor for selective access to stored data, a plurality of X write lines the control gate of each said storage transistor in a row of said memory cells being connected to an X write line corresponding to said row, a plurality of X sense lines the emitter of each said bipolar transistor in a row of said memory cells being connected to an X sense line corresponding to said row, a plurality of source lines the source of each said bipolar transistor in a row of said memory cells being connected to a source line corresponding to said row, and a plurality of Y sense lines the collector of each said bipolar transistor in a column of said memory cells being connected to a Y sense line corresponding to said column, the method characterized by the steps of:

(a) applying an erase voltage to each of said Y sense lines and, simultaneously, maintaining each of said X sense lines at said erase voltage, maintaining each of said X write lines at ground and applying said erase voltage to each of said source lines such that each of said storage transistors assumes a relatively negative threshold state; and

(b) applying a write voltage to selected X write lines while maintaining unselected X write lines at ground, and, simultaneously, maintaining selected Y sense lines at ground and unselected Y sense lines at an inhibit voltage which is less than said write voltage and maintaining each of said X sense lines at an intermediate voltage which is equal to or less than the base/emitter breakdown voltage of

said bipolar transistors such that the storage transistors of memory cells located at the intersections of said selected X write lines and said selected Y sense lines assume a relatively positive threshold state.

2. A method according to claim 1 characterized in that said erase voltage is about +20 volts.

3. A method according to claim 1 or 2 characterized in that said write voltage is about +20 volts.

4. A method according to claim 1, 2 or 3 characterized in that said inhibit voltage is about +10 volts.

5. A method according to any one of the previous claims characterized in that said intermediate voltage is about +5volts.

6. A method according to claim 1 to 5 characterized by the further steps of:

(a) maintaining a selected X sense line of a row of memory cells at ground and, simultaneously, maintaining unselected X sense lines and each of said Y sense lines at a read voltage such that memory cells connected to said selected X sense line and having storage transistors in said low threshold state are relatively less conducting and memory cells connected to said selected X sense line and having storage transistors in said high threshold state are relatively more conducting; and

(b) monitoring the relative conductance of memory cells connected to said selected X sens lines.

7. A method according to claim 6 characterized in that said read voltage is about +3 volts.

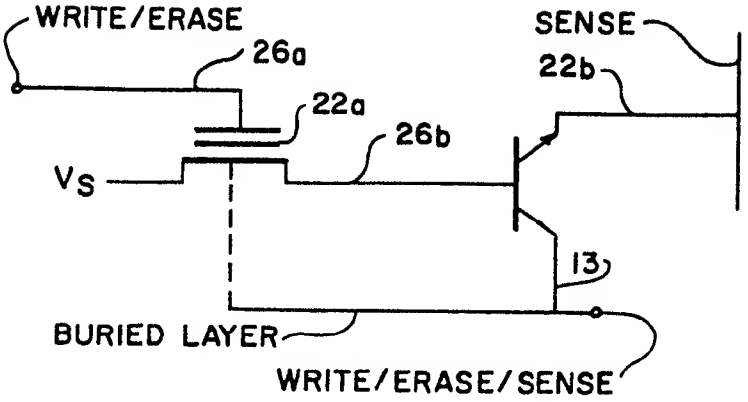
WRITE/ERASE
26a
22a
26b
VS
SENSE
22b
13
BURIED LAYER
WRITE/ERASE/SENSE

FIG. 1

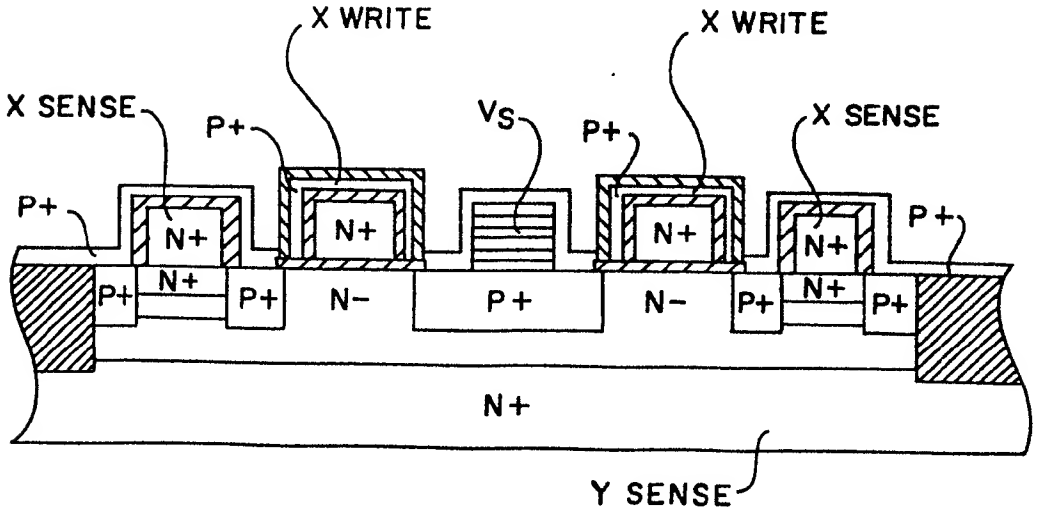
X WRITE
X WRITE
X SENSE
X SENSE
P+
VS
P+
P+
P+
N+
N+
N+
N+
P+
N+
P+
N-
P+
N-
P+
N+
P+
N+
Y SENSE

FIG. 4

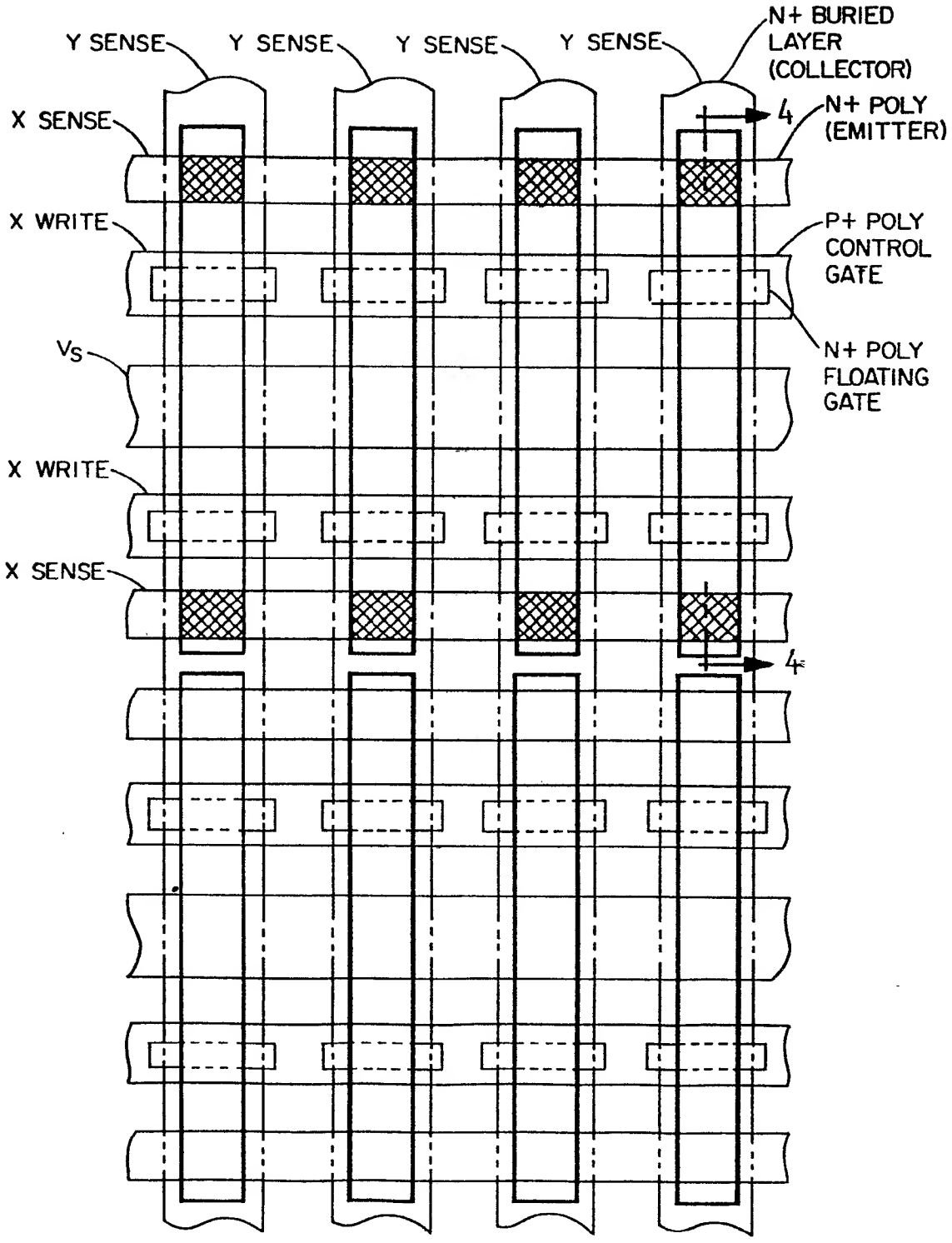
Y SENSE
Y SENSE
Y SENSE
Y SENSE
N+ BURIED LAYER (COLLECTOR)
X SENSE
4
N+ POLY (EMITTER)
X WRITE
P+ POLY CONTROL GATE
Vs
N+ POLY FLOATING GATE
X WRITE
X SENSE
4

FIG. 2

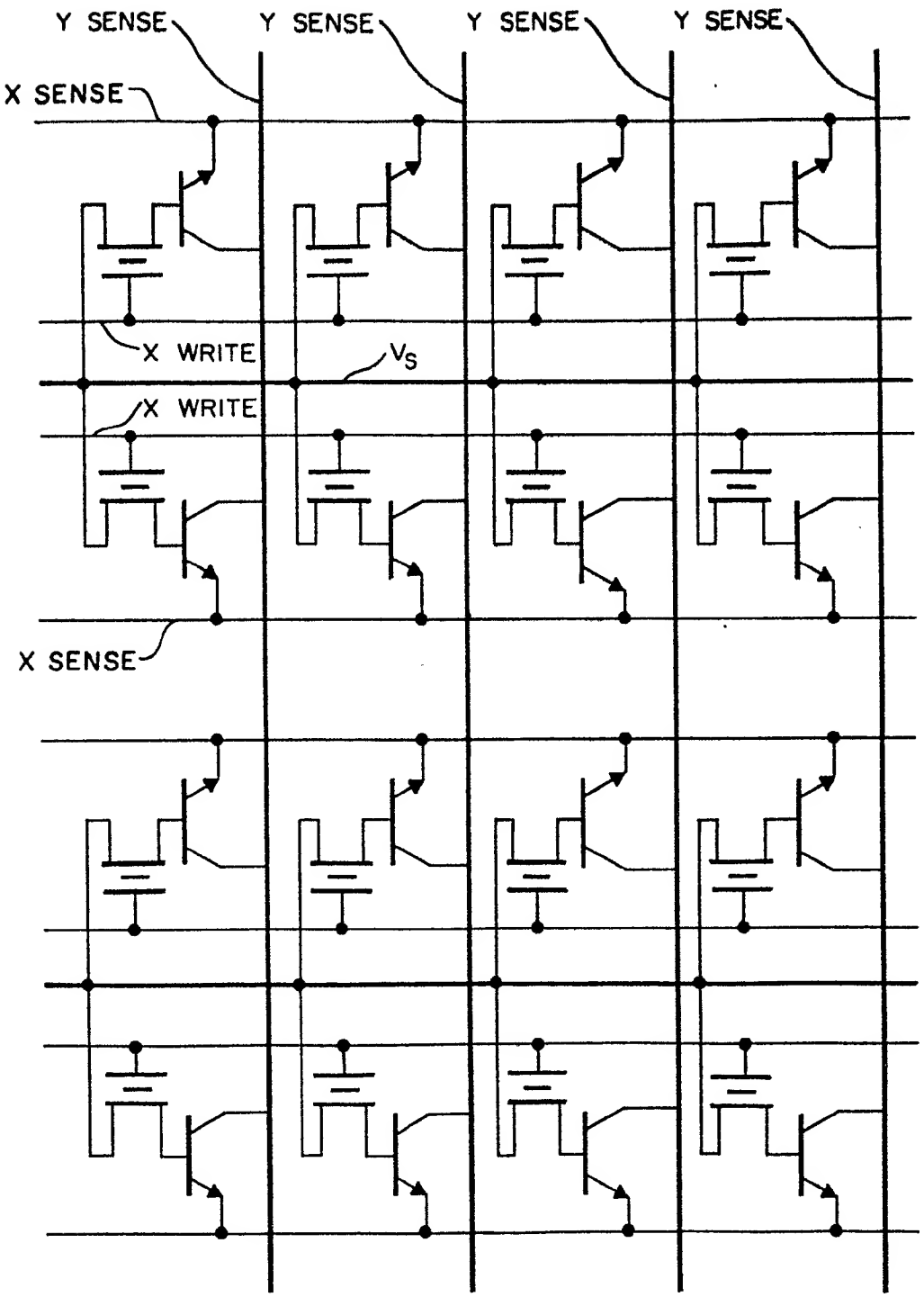
Y SENSE
Y SENSE
Y SENSE
Y SENSE
X SENSE
X WRITE
V_S
X WRITE
X SENSE

FIG. 3

European Patent Office

0176111

Application number

EP 85 11 2639

EUROPEAN SEARCH REPORT

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl 4)
A	US-A-3 893 085 (IBM) * Claims 2,5-9; column 3, line 27 - column 4, line 31; figures 1,3,4 *	1,6	G 11 C 17/00
A	FR-A-2 296 939 (NCR CORP.) * Claims 1,8; page 3, line 20 - page 4, line 24; figures 1-4 *	1	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 12, May 1980, pages 5296-5297, New York, US; D.M. KENNEY: "Bipolar erase technique in EPROM VMOS devices" * Page 5296, last paragraph - page 5297, paragraph 2; figure *	1	TECHNICAL FIELDS SEARCHED (Int. Cl 4) H 01 L G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20-01-1986	FRANSEN L.J.L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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